second portion 54b that is disposed over (vertically adjacent to) and insulated from the floating gate 38. A notch 68 is formed in the control gate 54 by the nitride spacer 52, which helps prevent reverse tunneling back to the floating gate or to the substrate. The non-volatile memory cell is of the split gate type as described in U.S. Patent No. 5,572,054, which discloses the operation of such a non-volatile memory cell and an array formed thereby, and is hereby incorporated herein by reference.

B. Please add the following new claims:

28. The device of claim 1, wherein:

the insulating layer first portion is formed directly against the floating gate, and the control gate is formed directly on the insulating layer first portion; and

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.

29. The device of claim 9, wherein:

the insulating layer first portion is formed directly against the floating gate, and the control gate is formed directly on the insulating layer first portion; and

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.